

Hierarchical Timing Analysis White Paper Cadence

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Hierarchical Timing Analysis White Paper WHITE PAPER Hierarchical Timing Analysis: Pros, Cons, and a New Approach By Pawan Gandhi, Naresh Kumar, Oleg Levitsky, Sharad Mehrotra, Ed Martinage, Brandon Bautz, Venkat Thanvantri, Prashant Sethia, and Ruben Molina, Cadence Design Systems, Inc. As digital semiconductor designs continue to grow larger, designers are looking to hierarchical Hierarchical Timing Analysis: Pros, Cons, and a New Approach A hierarchical approach lets designers be selective about the blocks they choose to analyze. Different Timing Models. The first methodology explored by the whitepaper is the Extracted Timing

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Model (ETM). These models replace some of the blocks in hierarchical timing analysis, providing a significant speed-up for full-chip analysis. Whitepaper: Hierarchical Timing Analysis Tradeoffs, and a ... Abstract: In this paper, we examine the impact of using the hierarchy of the design and multiple delay models defined at different abstraction levels to speed up the timing performance evaluation of VLSI circuits. The algorithms implemented in the Dynamic and Hierarchical Timing Analysis (DHTA) tool are described. Timing analysis speed-up using a hierarchical and a ... CiteSeerX - Document Details (Isaac Councill, Lee Giles, Pradeep Teregowda): We propose a hierarchical timing analysis technique for combinational circuits

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under the tightest known sensitization criterion, the XBD0 delay model. Given a hierarchical combinational circuit, a generalized delay model of each leaf module is characterized first. CiteSeerX — Hierarchical Functional Timing Analysis Hierarchical Functional Timing Analysis\u0003 Yuji Kukimoto Robert K. Brayton Department of Electrical Engineering and Computer Sciences University of California, Berkeley, CA 94720 fkukimoto,braytong@eecs.berkeley.edu Abstract We propose a hierarchical timing analysis technique for combinational circuits under the tightest known sensitization criterion, the XBD0 delay model. Given a ... Hierarchical functional timing analysis | 10.1145/277044 ... Given a

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Niall Campbell Ferguson (/ ' n i: l /; born 18 April 1964) is a Scottish-American historian and the Milbank Family Senior Fellow at the Hoover Institution at Stanford University. Previously, he was a professor at Harvard University and New York University, visiting

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